Section 26. Watchdog Timer and Sleep Mode

HIGHLIGHTS

This section of the manual contains the following major topics:

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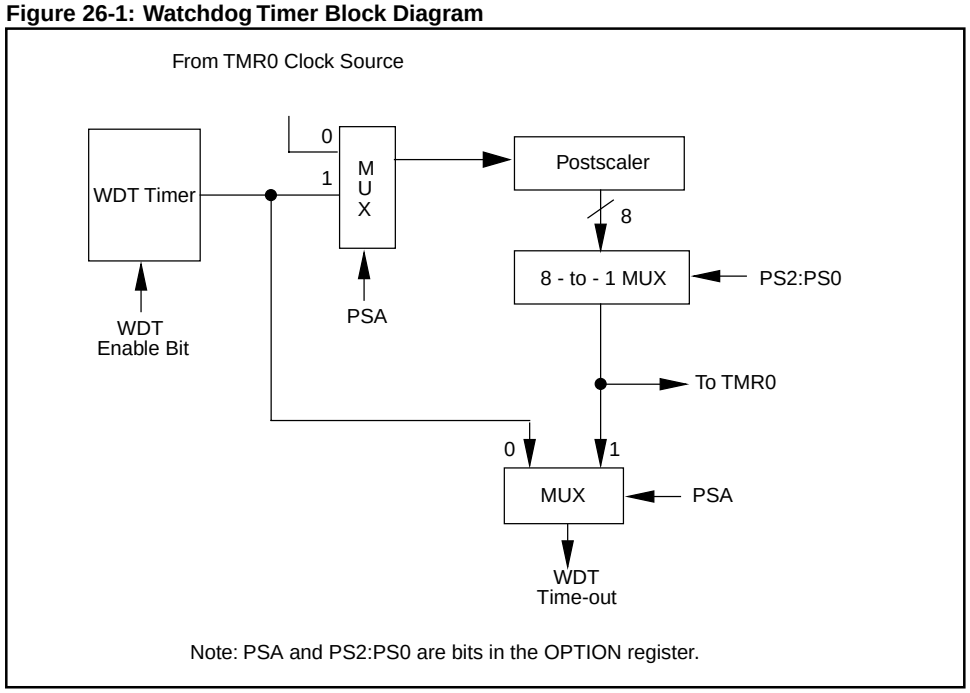
26.1 Introduction

The Watchdog Timer (WDT) is a free running on-chip RC oscillator which does not require any external components. The block diagram is shown in Figure 26-1. This RC oscillator is separate from the device RC oscillator of the OSC1/CLKIN pin. This means that the WDT will run, even if the clock on the OSC1 and OSC2 pins has been stopped, for example, by execution of a SLEEP instruction.

The Watchdog Timer (WDT) is enabled/disabled by a device configuration bit. If the WDT is enabled, software execution may not disable this function.

Figure 26-1: Watchdog Timer Block Diagram



Note: PSA and PS2:PS0 are bits in the OPTION register.

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26.2 Control Register

The OPTION_REG register is a readable and writable register which contains various control bits to configure the TMR0 prescaler/WDT postscaler, the External INT Interrupt, TMR0, and the weak pull-ups on PORTB.

Note:	To achieve a 1:1 prescaler assignment for the TMR0 register, assign the prescaler to the Watchdog Timer.

Register 26-1: OPTION_REG Register

R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1	R/W-1
$\overline{\text{RBPU}}$ (1)	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0
bit 7							bit 0

bit 7 **$\overline{\text{RBPU}}$ (1):** Weak Pull-up Enable bit
1 = Weak pull-ups are disabled
0 = Weak pull-ups are enabled by individual port latch values

bit 6 **INTEDG**: Interrupt Edge Select bit
1 = Interrupt on rising edge of INT pin
0 = Interrupt on falling edge of INT pin

bit 5 **T0CS**: TMR0 Clock Source Select bit
1 = Transition on T0CKI pin
0 = Internal instruction cycle clock (CLKOUT)

bit 4 **T0SE**: TMR0 Source Edge Select bit
1 = Increment on high-to-low transition on T0CKI pin
0 = Increment on low-to-high transition on T0CKI pin

bit 3 **PSA**: Prescaler Assignment bit
1 = Prescaler is assigned to the WDT
0 = Prescaler is assigned to the Timer0 module

bit 2:0 **PS2:PS0**: TMR0 Prescaler/WDT Postscaler Rate Select bits

Bit Value	TMR0 Rate	WDT Rate
000	1 : 2	1 : 1
001	1 : 4	1 : 2
010	1 : 8	1 : 4
011	1 : 16	1 : 8
100	1 : 32	1 : 16
101	1 : 64	1 : 32
110	1 : 128	1 : 64
111	1 : 256	1 : 128

Legend		
R = Readable bit	W = Writable bit	
U = Unimplemented bit, read as '0'		- n = Value at POR reset

Note 1:	Some devices call this bit $\overline{\text{GPPU}}$. Devices that have the $\overline{\text{RBPU}}$ bit, have the weak pull-ups on PORTB, while devices that have the $\overline{\text{GPPU}}$ have the weak pull-ups on the GP Port.

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26.3 Watchdog Timer (WDT) Operation

During normal operation, a WDT time-out generates a device RESET. If the device is in SLEEP mode, a WDT time-out causes the device to wake-up and continue with normal operation, this is known as a WDT wake-up. The WDT can be permanently disabled by clearing the WDTE configuration bit.

The postscaler assignment is fully under software control, i.e., it can be changed “on the fly” during program execution.

Note:	To avoid an unintended device RESET, the following instruction sequence (shown in Example 26-1) must be executed when changing the prescaler assignment from Timer0 to the postscaler of the WDT. This sequence must be followed even if the WDT is disabled.

In Example 26-1, the first modification of the OPTION_REG does not need to be included if the final desired prescaler is other then 1:1. If the final prescaler value is 1:1, then a temporary prescale value is set (other than 1:1), and the final prescale value is set in the last modification of the OPTION_REG. This sequence must be followed since the value in the TMR0 prescaler is unknown, and is being used as the WDT postscaler. If the OPTION_REG is changed without this code sequence, the time before a WDT reset is unknown.

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Example 26-1: Changing Prescaler (Timer0→WDT)

```
    BSF     STATUS, RP0    ; Bank1
    MOVLW   B’xx0x0xxx’    ; Select clock source and postscale value
    MOVWF   OPTION_REG     ;   other than 1:1
    BCF     STATUS, RP0    ; Bank0
    CLRF    TMR0           ; Clear TMR0 & Prescaler
    BSF     STATUS, RP0    ; Bank1
    MOVLW   B’xxxx1xxx’    ; Select WDT, do not change prescale value
    MOVWF   OPTION_REG     ;
    CLRWDT                 ; Clears WDT
    MOVLW   b'xxxx1xxx'    ; Select new prescale value and WDT
    MOVWF   OPTION_REG     ;
    BCF     STATUS, RP0    ; Bank0
```

To change prescaler from the WDT to the Timer0 module use the sequence shown in Example 26-2.

Example 26-2: Changing Prescaler (WDT→Timer0)

```
    CLRWDT                 ; Clear WDT and postscaler
    BSF     STATUS, RP0    ; Bank1
    MOVLW   b'xxxx0xxx'    ; Select TMR0, new prescale
    MOVWF   OPTION_REG     ; value and clock source
    BCF     STATUS, RP0    ; Bank0
```

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26.3.1 WDT Period

The WDT has a nominal time-out period of 18 ms, (with no postscaler). The time-out period varies with temperature, VDD and process variations from part to part (see DC specs). If longer time-outs are desired, a postscaler with a division ratio of up to 1:128 can be assigned to the WDT, under software control, by writing to the OPTION_REG register. Thus, time-out periods of up to 2.3 seconds can be realized.

The CLRWDT and SLEEP instructions clear the WDT and the postscaler (if assigned to the WDT) and prevent it from timing out and generating a device RESET.

The $\overline{TO}$ bit in the STATUS register will be cleared upon a Watchdog Timer time-out (WDT Reset and WDT wake-up).

26.3.2 WDT Programming Considerations

It should also be taken in account that under worst case conditions (VDD = Minimum, Temperature = Maximum, maximum WDT postscaler) it may take several seconds before a WDT time-out occurs.

Note:	When the postscaler is assigned to the WDT, always execute a CLRWDT instruction before changing the postscale value, otherwise a WDT reset may occur.

Table 26-1: Summary of Watchdog Timer Registers

Name	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Config. bits	MPEEN	BODEN	CP1	CP0	$\overline{PWRTE}$	WDTE	FOSC1	FOSC0
OPTION_REG	$\overline{RBPU}$	INTEDG	T0CS	T0SE	PSA	PS2	PS1	PS0

Legend: Shaded cells are not used by the Watchdog Timer.

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26.4 SLEEP (Power-Down) Mode

Sleep (Power-down) mode is a mode where the device is placed in it's lowest current consumption state. The device oscillator is turned off, so no system clocks are occurring in the device. Sleep mode is entered by executing a SLEEP instruction.

If enabled, the Watchdog Timer will be cleared but keeps running, the $\overline{PD}$ bit in the STATUS register is cleared, the $\overline{TO}$ bit is set, and the oscillator driver is turned off. The I/O ports maintain the status they had, before the SLEEP instruction was executed (driving high, low, or hi-impedance).

For lowest current consumption in this mode, all I/O pins should be either at V_{DD}, or V_{SS}, with no external circuitry drawing current from the I/O pin and the modules that are specified to have a delta sleep current should be disabled. I/O pins that are hi-impedance inputs should be pulled high or low externally to avoid switching currents caused by floating inputs. The T0CKI input should also be at V_{DD} or V_{SS} for lowest current consumption. The contribution from on-chip pull-ups on PORTB should be considered.

The $\overline{MCLR}$ pin must be at a logic high level (V_{IHMC}).

Some features of the device that consume a delta sleep current are enabled / disabled by device configuration bits. These include the Watchdog Timer (WDT) and Brown-out Reset (BOR) circuitry modules.

26.4.1 Wake-up from SLEEP

The device can wake-up from SLEEP through one of the following events:

1. Any device reset.
2. Watchdog Timer Wake-up (if WDT was enabled).
3. Any peripheral module which can set its interrupt flag while in sleep, such as:
   - External INT pin
   - Change on port pin
   - Comparators
   - A/D
   - Timer1
   - LCD
   - SSP
   - Capture

The first event will reset the device upon wake-up. However the latter two events will wake the device and then resume program execution. The $\overline{TO}$ and $\overline{PD}$ bits in the STATUS register can be used to determine the cause of device reset. The $\overline{PD}$ bit, which is set on power-up is cleared when SLEEP is invoked. The $\overline{TO}$ bit is cleared if WDT wake-up occurred.

When the SLEEP instruction is being executed, the next instruction (PC + 1) is pre-fetched. For the device to wake-up through an interrupt event, the corresponding interrupt enable bit must be set (enabled). Wake-up is regardless of the state of the GIE bit. If the GIE bit is clear (disabled), the device continues execution at the instruction after the SLEEP instruction. If the GIE bit is set (enabled), the device executes the instruction after the SLEEP instruction and then branches to the interrupt address (0004h). In cases where the execution of the instruction following SLEEP is not desirable, the user should have an NOP after the SLEEP instruction.

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26.4.2 Wake-up Using Interrupts

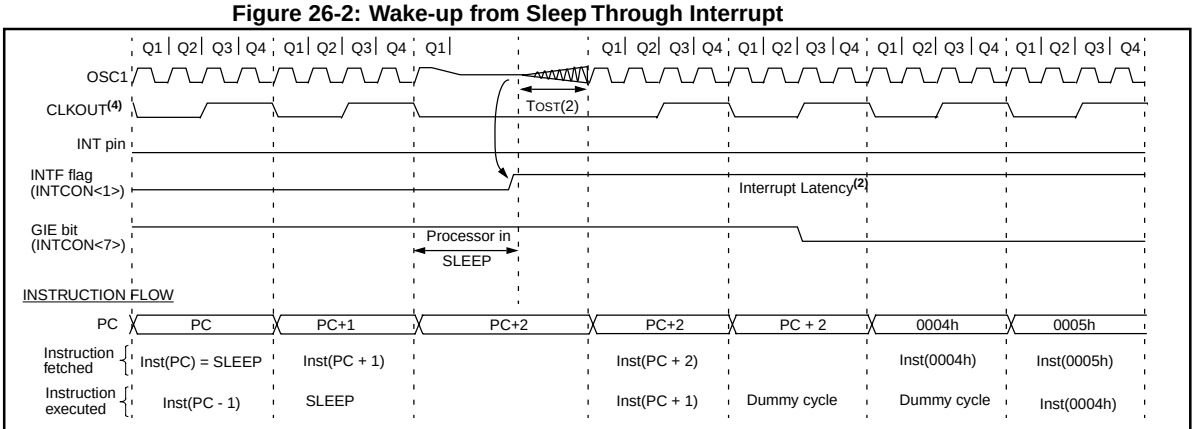
When interrupts are globally disabled (GIE cleared) and any interrupt source has both its interrupt enable bit and interrupt flag set, one of the following events will occur:

- If the interrupt occurs before the execution of a SLEEP instruction, the SLEEP instruction will complete as an NOP. Therefore, the WDT and WDT postscaler will not be cleared, the $\overline{TO}$ bit will not be set and $\overline{PD}$ bit will not be cleared.
- If the interrupt occurs during or after the execution of a SLEEP instruction, the device will immediately wake-up from sleep. The SLEEP instruction will be completely executed before the wake-up. Therefore, the WDT and WDT postscaler will be cleared, the $\overline{TO}$ bit will be set and the $\overline{PD}$ bit will be cleared.

Even if the flag bits were checked before executing a SLEEP instruction, it may be possible for flag bits to become set before the SLEEP instruction completes. To determine whether a SLEEP instruction executed, test the $\overline{PD}$ bit. If the $\overline{PD}$ bit is set, the SLEEP instruction was executed as an NOP.

To ensure that the WDT is clear, a CLRWDT instruction should be executed before a SLEEP instruction.

Figure 26-2: Wake-up from Sleep Through Interrupt



Note 1: XT, HS or LP oscillator mode assumed.
2: TOST = 1024TOSC (drawing not to scale) This delay will not be there for RC osc mode.
3: GIE = '1' assumed. In this case after wake- up, the processor jumps to the interrupt routine. If GIE = '0', execution will continue in-line.
4: CLKOUT is not available in these osc modes, but shown here for timing reference.

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26.5 Initialization

No initialization code at this time.

26.6 Design Tips

Question 1: ***My system voltage drops and then returns to the specified device voltage range. The device is not operating correctly and the WDT does not reset and return the device to proper operation.***

Answer 1:

The WDT was not designed to be a recovery from a brown-out condition. It was designed to recover from errant software operation (the device remaining in the specified operating ranges). If your system can be subjected to brown-outs, either the on-chip brown-out circuitry should be enabled or an external brown-out circuit should be implemented.

Question 2: ***Device resets even though I do the CLRWDT instruction in my loop.***

Answer 2:

Make sure that the loop with the CLRWDT instruction meets the minimum specification of the WDT (not the typical).

Question 3: ***Device never gets out of resets.***

Answer 3:

On power-up, you must take into account the Oscillator Start-up time (Tost). Sometimes it helps to put the CLRWDT instruction at the beginning of the loop, since this start-up time may be variable.

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26.7 Related Application Notes

This section lists application notes that are related to this section of the manual. These application notes may not be written specifically for the Mid-Range MCU family (that is they may be written for the Base-Line, or High-End families), but the concepts are pertinent, and could be used (with modification and possible limitations). The current application notes related to the WDT and Sleep Mode are:

Title	Application Note #
Power-up Trouble Shooting	AN607

26.8 Revision History

Revision A

This is the initial released revision of the Watchdog Timer and Sleep mode description.

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